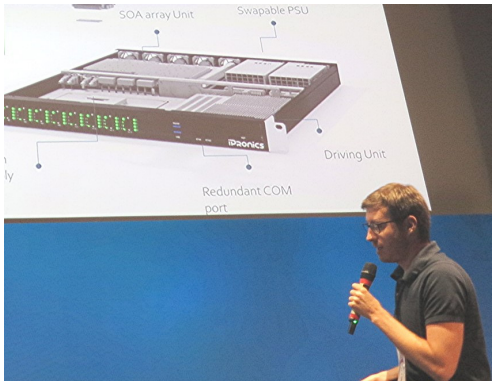
Leti Innovation Days, June 17–19, 2025, Grenoble, France

The optical interconnect technology will be used more and more in modern data centers where the servers have to handle artificial intelligence (AI) which strongly increases the huge amount of data. AI applications drive the need for scaling the interconnect bandwidth to cope with the large-scale AI model size for training and inference. AI large language models (LLMs) require rapid processing of large datasets, which demands significant computational power and leads to high energy consumption. Modern AI datacenter (or AI factory) has massive numbers of GPUs (100,000–200,000 or more) in a training cluster. Some of the largest data centers being planned today are projecting 300–1000 MW of power (where roughly 8% of the MW is attributable to optical network). Scale-out and AI density depend on optical connectivity in order to obtain high bandwidth, low latency and low power consumption, and this drive new integration schemes with co-packaged computing and electro-optical chiplets. Data travels faster in optical interconnects than in traditional electrical connections, which results in lower latency and lower power consumption in the different parts of the AI cluster. Silicon photonics-based transceivers offer significant potential for improving the efficiency of data transfer within local GPU accelerators. By integrating electrical and photonic integrated circuits (PICs) in a 2.5D or 3D IC package, these transceivers can facilitate die-to-die communication with the GPU through very low power and parallel dense electrical interfaces. These new kind of optical chiplets, can significantly increase energy savings for large data transfers by removing copper connections, making it a crucial technology for the future of high-performance computing and data centers. For example among others represents ST Microelectronics' silicon photonic PIC100 technology a cutting-edge advancement in this new class of optical communications and integrated photonics.

CEA-Leti has developed a solution for on board interconnect with highly parallel optical data communication using µLED/µphotodiode GaN array technology which enables interconnects with very high data rate and density (>10Tbp/s/mm^2), low power consumption at 0.5 pJ/bit and low latency. Compared to the traditional silicon photonics serial link has the new parallel link x10 energy efficiency gain. The STARAC demonstrator from Leti is using chiplets on a photonic interposer.

AI and generative AI can be very useful making many applications and functions more efficient. This technology will be able make many operations more optimal, such as more efficient tools, more efficient equipment, new system architectures and innovation etc. AI is in many ways the defining technology for the electronics industry and there are huge investments of this technology in industry, R&D and government institutions.

Denis Dutoit, program manager, CEA-List. The STARAC demonstrator uses chiplets on photonic interposer, and the Chiplet architecture co-optimization with silicon photonics and 3D integration enables high bandwidth, low latency and low power interconnects



Daniel Pérez López, founder & CTO, iPRONICS. We design reconfigurable high speed, gain-controlled optical switches in compact 1U and 2U sizes to AI data centers.

Ashkan Seyedi, director, optical interconnect, NVIDIA. There are many GPUs in modern AI data-centers, e.g. has Elon Musk' Colossus training cluster 200,000 GPUs or more.

Giorgio Cazzaniga, senior director Jabil Photonics. Co-package optics (CPO) are important and enable less power consumption, reduced latency and less cost/bit. Jabil delivers silicon photonics PIC from prototyping to large scale manufacturing.

Anthony Mastroianni, senior director, 3D-IC solutions, Siemens EDA. Design of co-package optics (CPO) requires co-design and co-optimization approaches which our advanced 3D-IC co-design platform, Innovator, enables.

Photonics panel discussion (from left) Daniel Pérez López, Ashkan Seyedi, Giorgio Cazzaniga, Denis Dutoit, Anthony Mastroianni

Jean-René Lèquepeys, CTO, CEA-Leti. While optical interconnections are adressing the HPC and AI challenges in data centers, memory scaling is also needed in AI applications, e.g. with in-memory computing with vertical memories in 3D stacks. It gives x100 energy efficiency gain.